ABSTRACT OF THE DISCLOSURE

Apparatus and method are provided for eliminating stalls in read and write operations to a data cache within a multi-streaming microprocessor core. The apparatus provides a multi-streaming microprocessor core, for executing instruction streams running within the multi-streaming microprocessor core at any time. The multi-streaming microprocessor core includes instruction queues, a bypass structure, and address matching logic. The instruction queues each correspond to each of the instruction streams. The each of the instruction queues has first instructions, store instructions, and load instructions. The first instructions are for dispatch to one or more functional units. The store instructions are for dispatch to a data cache, wherein the store instructions direct write operations. The load instructions are for dispatch to the data cache, where the load instructions direct read operations. The bypass structure is within the data cache. The bypass structure receives the store instructions and has multiple elements. If the write operations hit in the data cache, data corresponding to the write operations are stored in one or more of the elements in the bypass structure before the data is written to the data cache. The address matching logic is coupled to the bypass structure within the data cache. The address matching logic receives the load instructions, where the read operations use the address matching logic to search the elements of the bypass structure to identify and use any one or more of the elements representing more recent data than that stored in the data cache.